

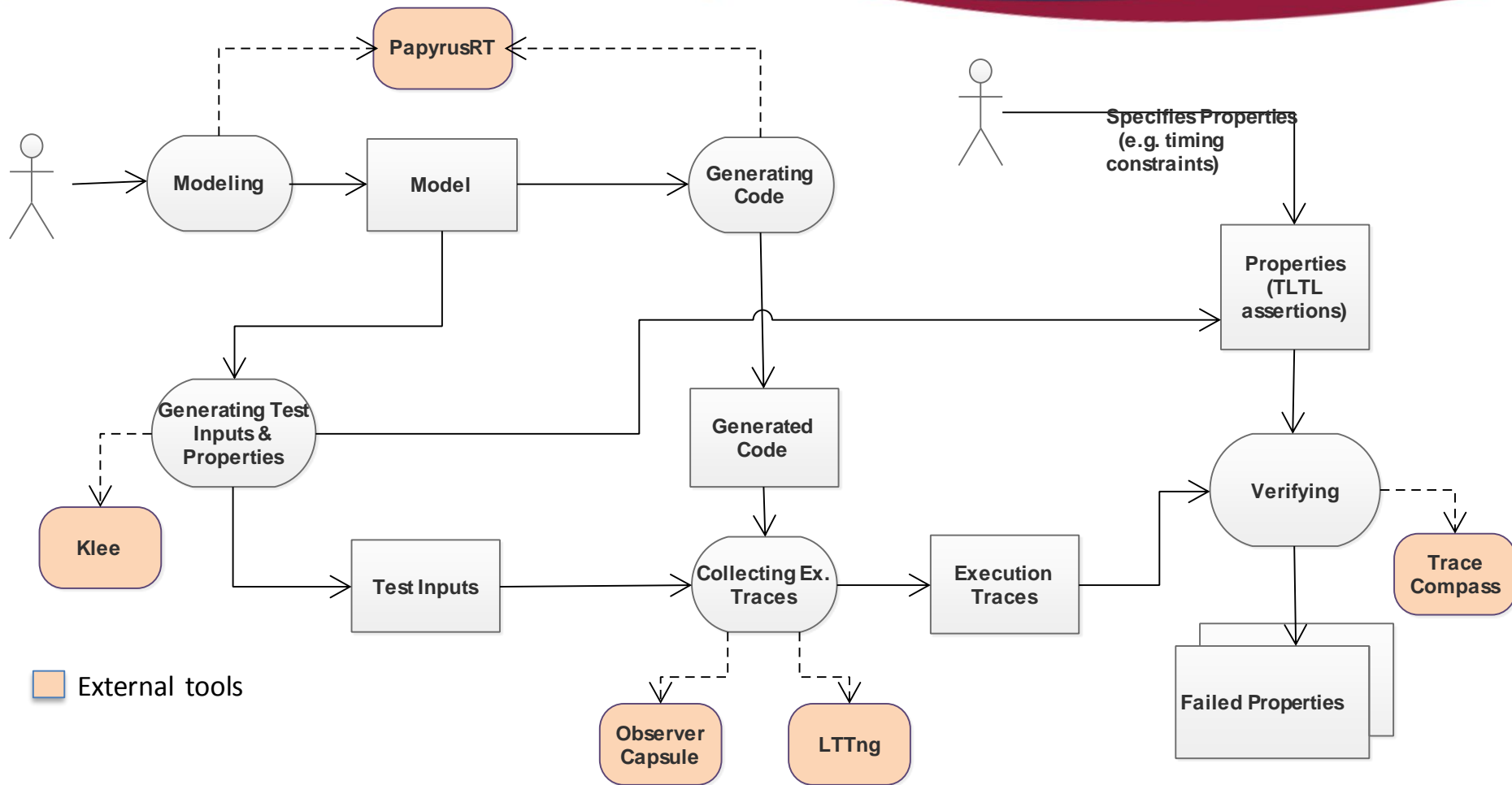


# Run-time Verification of Models of Real-Time Embedded Systems

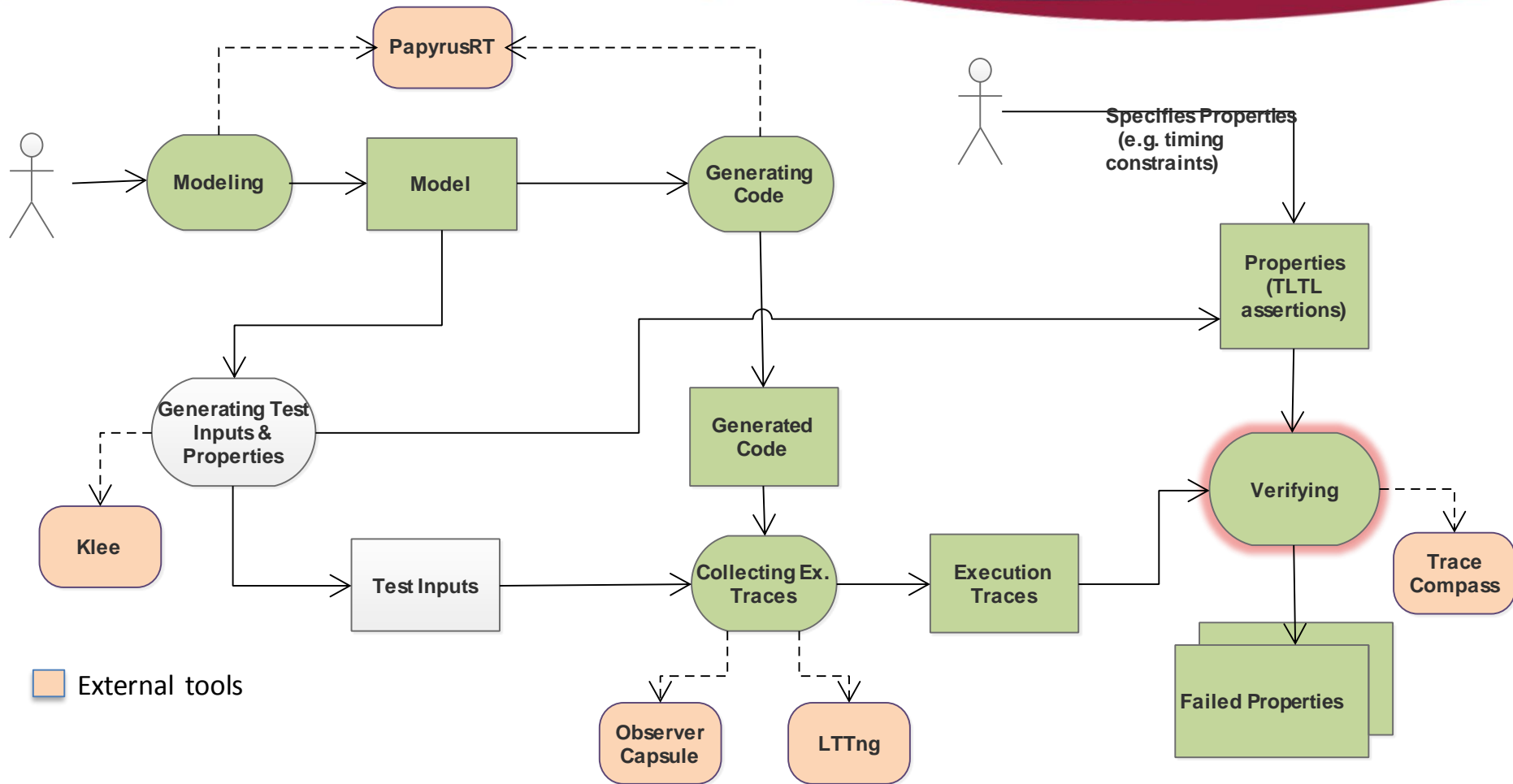
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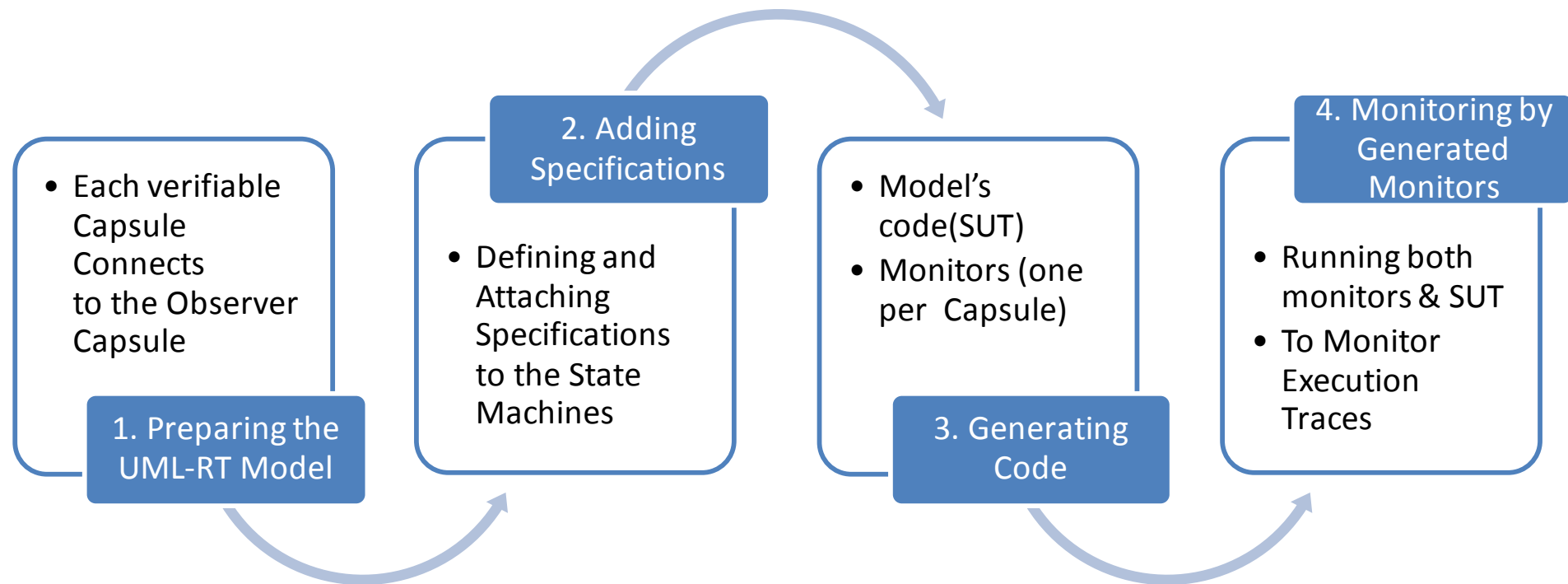
# An Automatic Solution for Runtime Verification of UML-RT Models



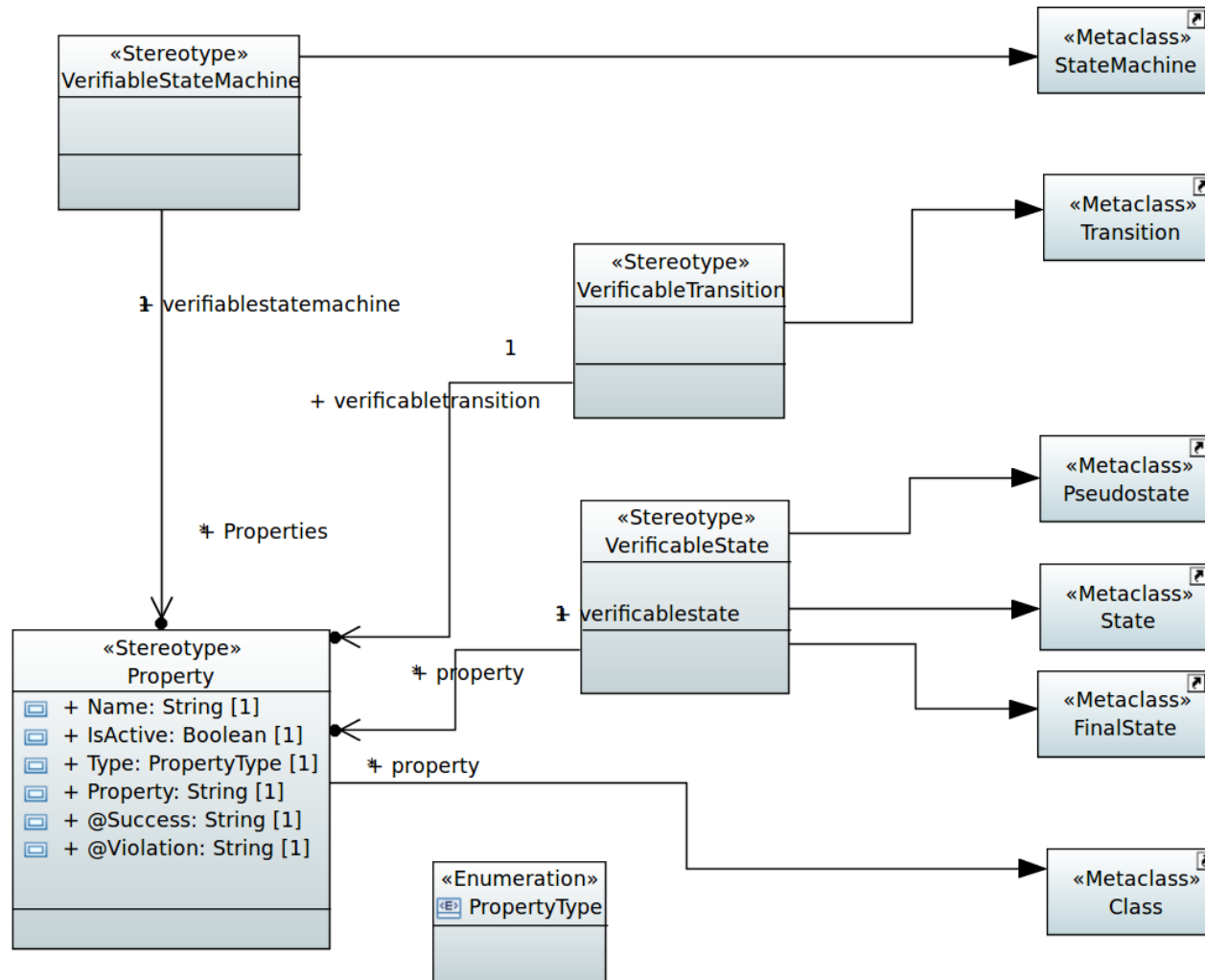
# Our Verifier that Works with State-of-the-art



# Verifying Simple Timing Constraint Properties in Papyrus-RT: Steps



# State Machine Stereotypes as Specifications



# Generating & Verifying Simple Timing Constraints on a Rover



# Summary & Future Work

- ✓ Specifying Simple Timing Constraint Properties on State Machines
- ✓ Generating Monitors for State Machine Properties Using Our Monitor Generator
- ✓ Verifying Properties on the Rover
- + Advanced Properties on a More Complex Rover
  - E.g. Running Plans by the Rover and Checking Related Temporal Properties
- + Test Input & Property Generation
  - An automatic end to end runtime verification solution